Q.P. Code – 42244

Second Semester B.Sc. Degree Examination, April/May 2019

(CBCS Scheme)

Electronics

Paper II – LINEAR AND DIGITAL INTEGRATED CIRCUITS

Time : 3 Hours] *[Max. Marks : 90*

Instructions to Candidates : Answers any Ten questions from Part A, any Five questions from Part B, any Five questions from Part C and any Five questions from Part D.

PART – A

Answer any **TEN** questions : **(10 × 1 = 10)**

1. Write the equivalent circuit of op-amp.
2. What is differentiator?
3. Mention one application of open-loop configuration of op-amp.
4. For a feedback to be negative. What should be the phase difference between input and output?
5. Write the expression for voltage gain of a FET C.S. amplifier.
6. Draw the equivalent circuit of UJT.
7. Name the digital code used in k-map cell representation.
8. Write the expression for carry of a full adder.
9. Mention the IC for BCD to decimal decoder.
10. What is the value of output Q of a RS flipflop if preset = 0, R = 1 and S = 0?
11. Mention the disadvantages of binary weighted resistor DAC.
12. What is the value of maximum count of a 6-bit counter?

PART – B

Answer any **FIVE** questions. **(5 × 8 = 40)**

13. (a) Mention any four characteristics of ideal op-amp. Give any two drawbacks of open-loop configuration of op-amp.

    (b) What is integrator? Draw the circuit of op-amp integrator and derive an expression for its output voltage. **(4 + 4)**

14. (a) Draw the circuit diagram of phase shift oscillator. Explain its working and write the expression for frequency of oscillation.

    (b) What is zero crossing detector? With circuit diagram and waveforms explain the working of zero crossing detector. **(4 + 4)**

15. (a) With circuit diagram explain the working of two stage RC coupled amplifier. Also draw its frequency response.

    (b) Write the block diagram representations for four types of negative feedback connections. Mention the advantages of negative feedback. **(4 + 4)**

16. (a) With circuit diagram, explain the working of Hartley oscillator. Write the expression for frequency of oscillation.

    (b) With circuit diagram, explain the working of UJT relaxation oscillator. Write the expression for frequency of oscillation. **(4 + 4)**

17. (a) What is full subtractor? Write its truth table and obtain the expression for its outputs.

    (b) What is magnitude comparator? Draw the circuit of a 2 bit comparator for equality output and explain the process of comparison. **(4 + 4)**

18. (a) What is demultipelxer? Write the truth table and expressions for output of a 1 : 4 demux. Draw the logic diagram.

    (b) Draw the logic diagram of BCD to seven segment decoder/driver. Explain the functionalities of pins $\overline{LT}$, $\overline{RBI}$. **(4 + 4)**

19. (a) Draw the circuit diagram of master slave JK flipflop using NAND gates and explain the working of master slave JK flip flop.

    (b) Draw the logic diagram of a 4-bit parallel in serial out shift register and explain its working. **(4 + 4)**

20. (a) With the schematic diagram, explain the working of successive approximation analog to digital converter.

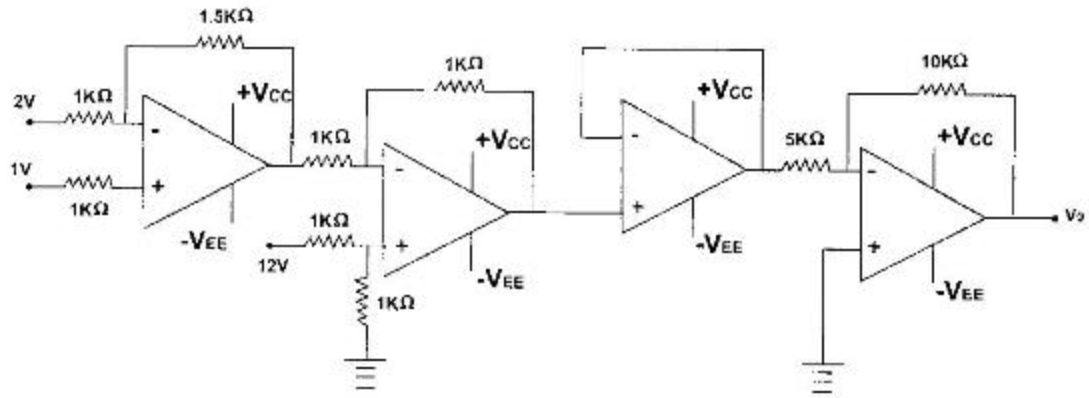
    (b) What is VCO? Draw the circuit diagram of VCO using IC 555 and explain its working. **(4 + 4)**

PART C

Answer any **FIVE** questions :. **(5 × 6 = 30)**

21. Design a first order Butterworth high pass filter for a pass band gain of 5 and cutoff frequency of 5 kHz. Assume C = 0.1 μF and R_F = 10 kΩ. Calculate the magnitude of gain for frequencies (a) 1 kHz and (b) 10 kHz.

22. What is the output voltage in the following circuit? Assume V_{CC} = + 15 V and $-V_{EE}$ = - 15 V.



23. An amplifier has a mid frequency gain of 40 dB and frequency response from 500 Hz to 5 kHz. Determine the gain and bandwidth for a negative feedback amplifier. Given $\beta = 0.02$.

24. A Colpitt's oscillator is constructed using C_2 = 10 PF and C_1 = 100 PF capacitors and 10 mH inductor. Calculate the minimum gain required for the oscillations and frequency of oscillation. Also calculate the change in frequency of oscillation, if the value of inductor is increased by 20%.

25. Using K-map, simplify the Boolean function and realize the simplified expression using basic gates.

$$F = \sum m(0, 1, 5, 8, 9, 10, 13) + d(2, 11, 15)$$

26. (a) Realize the Boolean function $F = \sum m(0, 1, 2, 7, 9, 14)$ using multiplexer.

(b) Realize the Boolean functions $F_1 = \sum m(0, 1, 11)$ and $F_2 = \sum m(5, 9, 11, 12)$ using demultiplexer. **(3 + 3)**

27. Design an astable multivibrator using 555 timer for a frequency of 4 kHz. Given C = 0.1 μF and R_1 = 10 kΩ. Calculate the ON period and OFF period, also calculate the duty cycle. Draw the circuit diagram.

PART D

Answer any **FIVE** questions : **(5 × 2 = 10)**

28. BJT is a current driven device whereas FET is voltage driven. Justify.

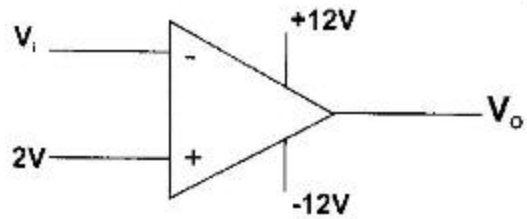
29. Among slew rate of 10 V/ μ s and 0.5 V/ μ s which one is preferred and why?

30.. Convert the given SOP to canonical form $Y = A + BC'$.

31. When a decade counter is turned ON, it has entered a invalid state 1100. What is the output for two clock cycles?

32. How to reduce the duty cycle of a astable multivibrator to less than 50%?

33. What is the output voltage of the following circuit for (a) $v_i = 1$ V (b) $v_i = 3$ V.



34. What is the output frequency of the following circuit?